Notice of Allowability	Application No.	Applicant(s)	
	10/786,401	KAMMLER ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 9/27/2005*.

2. ☒ The allowed claim(s) is/are *1-3,5-25,27-30 and 36-40*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Response to Amendment

1. Applicant's explanation of the instant invention in pointing the difference with the cited prior art was found to be persuasive.

EXAMINER'S AMENDMENT

2. In view of the allowable subject matter, the Applicant's representative was contacted to clarify the limitations of several claims.

3. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with J. Mike Amerson on October 13, 2005.

The application has been amended as follows:

In claim 22, line 16, following the word "process", - - of at least said second sidewall spacer - - was inserted.

In claim 23, line 2, following the phrase ". . material on said", "layer of first dielectric material" was deleted and - - gate electrode - - was inserted instead.

In claim 24, line 2, following the phrase ". . depositing a layer", "of said" was deleted and - - comprised of said - - was inserted.

In claim 24, line 3, following the phrase ". . etching said", "first dielectric layer" was deleted and - - deposited layer - - was inserted.

In claim 36, line 4, following the phrase ". . said recessed first", the word "side" was deleted and - - sidewall - - was inserted.

In claim 37, line 9, following the phrase ". . material on said", "layer of first dielectric material" was deleted and - - gate electrode - - was inserted instead.

In claim 37, line 12, following the phrase ". . first dielectric material", - - of at least said second sidewall spacer - - was inserted.

In claim 38, line 13, following the phrase ". . first dielectric material", - - of at least said second sidewall spacer - - was inserted.

In claim 40, line 10, following the phrase ". . first dielectric material", - - of at least said second sidewall spacer - - was inserted.

Allowable Subject Matter

4. Claims 1 – 3, 5 – 25, 27 – 30 and 36 – 40 are allowed.

5. The following is an examiner's statement of reasons for allowance:

Claims 1 – 3 and 5 – 9 recite, inter alia, a method, comprising the steps of forming a recessed first sidewall spacer adjacent to a polysilicon sidewall line formed above a substrate exposing an upper sidewall portion of the polysilicon line, forming a second sidewall spacer comprised of silicon dioxide adjacent to the first sidewall spacer by depositing a silicon dioxide layer over the polvsilicon line and the first recessed sidewall spacer and anisotropically etching the silicon dioxide layer reducing the size of said second sidewall spacer by a selective etch process to expose the upper sidewall portion and forming a metal silicide region on the exposed upper sidewall portion. The art of record does not disclose or anticipate the above limitation in

combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Claims 10 – 21 recite, inter alia, a method, comprising the steps of forming a silicon dioxide liner on sidewalls of a polysilicon line formed above a silicon region, forming a recessed first sidewall spacer on the silicon dioxide liner, said first sidewall spacer being comprised of a material that may be selectively etched with respect to silicon dioxide, forming a silicon dioxide sidewall spacer adjacent to said first sidewall spacer and selectively removing said silicon dioxide laver at least on portions of the polysilicon line not covered by the first sidewall spacer. The art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Claims 22 – 25 and 27 – 30 recite, inter alia, a method of forming a field effect transistor comprising the steps of forming a gate electrode on a gate insulation layer on a semiconductor material, forming a first recessed sidewall spacer, comprising at least a layer of a first dielectric material in contact with said gate electrode, and a second sidewall spacer comprised of the first dielectric material, forming a source/drain region, selectively removing a portion of the first dielectric material to substantially completely expose an upper sidewall portion of the gate electrode and forming a metal/ semiconductor compound region in the gate electrode, wherein the source/drain regions are completely exposed by an isotropic selective etch process of the second sidewall spacer prior to forming the metal/semiconductor compound region. The art of record

does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Claim 36 recites, inter alia, a method, comprising the steps of forming a recessed first sidewall spacer adjacent to a sidewall of a polysilicon line formed above a substrate, said first sidewall spacer exposing an upper sidewall portion of the polysilicon line, wherein forming said recessed first sidewall spacer comprises the steps of forming a conformal silicon dioxide layer on said polysilicon line, depositing a silicon nitride layer over said polysilicon line, and anisotropically etching said silicon nitride layer Iintil said upper sidewall portion is exposed, forming a second sidewall spacer adjacent to the first sidewall spacer, said second sidewall spacer having a predefined etch selectivity with respect to said polysilicon line and said substrate, reducing the size of the second sidewall spacer by a selective etch process according to said predefined etch selectivity so as to expose the upper sidewall portion and forming a metal silicide region on the exposed upper sidewall portion. The art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Claims 36 – 39 recite, inter alia, a method of forming a field effect transistor comprising the steps of forming a gate electrode on a gate insulation layer above a semiconductive material, forming a first recessed sidewall spacer and a second sidewall spacer, both first and second sidewall spacers comprise first dielectric material, forming a source/drain region, selectively removing a portion of the first dielectric material of the

second spacer to substantially completely expose the upper sidewall portion of the gate electrode and forming a metal/semiconductor compound region in the gate electrode. The art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Claim 40 recites, inter alia, a method of forming a field effect transistor comprising the steps of forming a gate electrode on a gate insulation layer above a semiconductive material, forming a first recessed sidewall spacer and a second sidewall spacer, both first and second sidewall spacers comprise first dielectric material silicon nitride, forming a source/drain region, selectively removing a portion of the first dielectric material of the second spacer to substantially completely expose the upper sidewall portion of the gate electrode and forming a metal/semiconductor compound region in the gate electrode. The art of record does not disclose or anticipate the above limitation in combination with other claim elements nor would it be obvious to modify the art of record so as to form a device including the above limitation.

Conclusion

6. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

8. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar
Asok K. Sarkar
October 13, 2005

Primary Examiner